III / SEM / E & TC / 2019 (S) [10-06-19, BACK-REG]

DIGITAL ELECTRONICS

Sub Code – **ETT-302**

Full Marks: 80 Time: 3 hours

Answer any **FIVE** questions including Q. No1 & 2

The figures in the right-hand margin indicate marks

1. Answer ALL Questions : **[2 x 10 = 20]**

(a) Convert $(25.75)_{10}$ into binary number and $(110111.10101111)_2$ into hexadecimal number.

(b) Define Radix of a number system.

(c) Convert the following Binary numbers into Gray codes: (I) 1101011 (II) 100010110

(d) State De-Morgan's theorem.

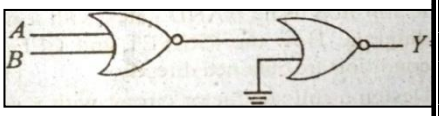
(e) Perform 1's complement subtraction of 00010 - 001111.

(f) Write down the truth table& symbol of 2-input Ex-NOR gate.

(g) Define fan-in and fan-out.

(h) Draw 2-input TTL NAND gate?

(i) What is the output of the following logic circuit? →



(j) Define half substractor and full substractor.

2. Answer any SIX Question: **[5 x 6 = 30]**

(a) Perform BCD addition of (204.6 + 185.56).

(b) What are universal gates and how the other gates can be implemented by universal gates?

(c) Simplify the Boolean expression y = $\overline{(A\bar{B}C)\left(\overline{A\bar{B}}\right)+\ BC}$ and draw the logic circuit using NAND gates only.

(d) Using K-map, obtain minimum sum of product for the switching function given by f (X, Y, Z, W) = Σ m (0, 1, 3, 7, 8, 12) + Σd (5, 10, 13, 14) and implement using AOI gates.

(e) Differentiate between combinational and sequential logic circuit.

(f) Design the operation of full adder with the help of truth table and circuit diagram.

(g) Design a 3:8 decoder with neat circuit diagram?

3. Define multiplexer and de-multiplexer. Explain the function of 4:1 MUX with neat logic diagram & truth-table. **[10]**

4. Design a 2 bit magnitude comparator circuit whose outputs are A > B, A = B, A < B, where A and Bare 2-bit numbers. **[10]**

5. Differentiate between Latches & Flip Flops. Explain the function of RS flip-flop & JK flip-flop with diagram& its functional table. **[10]**

6. Define Counter. With a suitable logic diagram design a decade counter. Write its truth table. **10]**

7. What are the various methods used for D/A conversion? Explain the working of aR-2R ladder network type D/A converter. **[10]**

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Collected By:-

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III / SEM / E & TC / 2019 (S) [10-06-19, BACK-EX-REG]

DIGITAL ELECTRONICS

Sub Code – **ETT-302**

Full Marks: 70 Time: 3 hours

Answer any **FIVE** Questions

The figures in the right-hand margin indicate marks

1. (*a*) Define weighted and non-weighted code. 2

(*b*) Subtract $(1010100)_2$ from $(1010110)_2$ using 2's complement. 5

(*c*) Define Excess-3 code. Convert the following : 7

$$(C3A{\cdot}47)_H \rightarrow (\ ?\ )_8 \rightarrow (\ )_2$$

2. (*a*) Draw the logic symbol and Truth Table of EX-NOR gate. 2

(*b*) Design EX-OR, EX-NOR gate from NOR gate. 5

(*c*) Draw the K-map for the boolean expression and relative using universal gates. 7

$$F(a, b, c) = \Sigma m\ (1, 2, 3, 6, 7)$$

3. (*a*) Define SOP and POS. 2

(*b*) Expand $A(A + B)(A + B + C)$ to Maxterms and Minterms. 5

(*c*) Reduce using the mapping the expression and relative using AOI gates

$$F(p, q, r, s) = \Sigma m(0, 1, 2, 3, 5, 7, 8, 9, 10, 12, 13)$$ 7

4. (*a*) Define Racing in sequential circuit. 2

(*b*) Explain Logic circuit, Gate level circuit, truth table and application of Full Adder. 5

(*c*) Explain working of simple 4 : 1 Multiplexer and 1 : 4 Demultiplexer with gate level circuit. 7

5. (*a*) State CMOS and ECL Logic Family. 2

(*b*) Explain briefly propagation Delay, Fan-out, Fan-in, Power Dissipation and Noise margin. 5

(*c*) Explain clocked JK Flip-flop with the help of level circuit logic circuit and truth table. 7

6. (*a*) Define PISO and PIPO. 2

(*b*) Explain the working of 4-bit Universal Shift Register. 5

(*c*) Explain the working of Synchronous Decade Counter with a neat diagram. 7

7. (*a*) State applications of shift Registers. 2

(*b*) Explain LED driver using IC 7447 decoder. 5

(*c*) Explain the performance parameters of DAC IC Resolution, Accuracy and Conversion time. 7

III / SEM / E & TC / 2018 (W) [DEC,REG]

DIGITAL ELECTRONICS

Sub Code – **ETT-302**

Full Marks: 80 Time: 3 hours

Answer any **FIVE** questions including Q. No1 & 2

The figures in the right-hand margin indicate marks

1) Answer the following questions briefly: - [2 x 10 = 20]

a) What is the difference between the weighted and non weighted codes? Give at least the example of each code?

b) Convert (11100101) Gray code to Binary.

c) Perform 2's complement subtraction of (12-15).

d) Define the radix of the number system?

e) Perform the BCD addition of (204.6+185.56).

f) Define racing condition?

g) State De-Morgan's theorem?

h) Write down the truth table of 2 inputs Ex-OR gate?

i) Define modulus of counter?

j) Question is not been mentioned

2) Answer any six of the following questions: - [5 x 6 = 30]

a) Which gates are referred as universal gates and why? How other gates can be realized using NAND gates?

b) Differentiate between combinational and sequential logic circuits.

c) Describe the operation of full substractor with the help of truth table and circuit diagram?

d) Simplify the Boolean expression Y = [AB(C+BD) +A. B]C

e) Simplify the given expression using Karnaugh's map and draw the logic circuit using universal gates? $F(A,B,C,D) = \sum m(1,4,5,8,9,10) + d(3,11,13)$

f) Draw the operation of seven segment display?

g) Write down the difference between synchronous and asynchronous counters?

3) With a neat circuit diagram explain the function of 4:1 MUX and 1:4 De-MUX. [10]

4) Design a 2 bit magnitude comparator circuit whose outputs are P > Q, P < Q and P = Q where P and Q are 2 bit numbers. [10]

5) Sketch the logic diagram of clocked JK flip flop and explain its working with a functional table.

6) With neat diagram explain 4 bit ripple counter with its wave forms. [10]

7) Describe the operation of SISO and SIPO register with proper diagram. [10]

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Collected By:-
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III / SEM / E & TC / 2018 (W) [DEC, EX-REG]

DIGITAL ELECTRONICS

Sub Code – **ETT-302**

Full Marks: 70 Time: 3 hours

[Answer any **FIVE** Questions]

The figures in the right-hand margin indicate marks

1)

(a) What is radix of a number? **[2]**

(b) Subtract $(37)_{10}$ from $(25)_{10}$ using 2's complement and 1's complement subtraction. **[5]**

(c) Which gates are known as universal logic gates? Realize other gates using one of the universal gates. **[7]**

2)

(a) What is an ASCII code? **[2]**

(b) State and prove de-Morgan's theorem. **[5]**

(c) Using K-map solve: - $F(A,B,C,D)=\sum(0,1,3,7,8,12)+\sum d(5,10,13,14)$. Implement results using AOI gate **[7]**

3)

(a) What is the difference between combinational logic and sequential logic circuits? **[2]**

(b) Design full adder circuit with neat diagram. **[5]**

(c) Design a 2 bit magnitude comparator. **[7]**

4)

(a) What is resistor and where is it used? **[2]**

(b) Design a 4:1 MUX with a neat circuit diagram. **[5]**

(c) Explain the working of clocked S-R flip flop using NAND gates. **[7]**

5)

(a) What is fan in and fan out? **[2]**

(b) Explain working of 2 input TTL NAND gate. **[5]**

(c) Simplify the Boolean expression by Boolean algebra & draw logic circuit using NAND gate.

6)

(a) What is a modulus of a counter? **[2]**

(b) Explain working of 4 bit SISO register with a neat diagram. **[5]**

(c) Define a 4 - bit ripple counter with a neat diagram. **[7]**

7)

(a) What is resolution of DAC? **[2]**

(b) Explain the RAMP type ADC with a neat diagram. **[5]**

(c) Explain R-2R Ladder DAC with neat diagram and give its advantages. **[7]**

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Collected By:-

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III-SEM/E&TC/AE&I/2018 (S) [17-05-2018, BACK]

DIGITAL ELECTRONICS

Sub Code – **ETT-302**

Full Marks: 70

Time: 3 hours

Answer any **FIVE** Questions

The figures in the right-hand margin indicate marks

1. **(a)** Add 562 from 357 by using BCD addition method. **[2]**

(b) Which gates are referred to as Universal gates and how other gates can be realized using NOR gates only? **[5]**

(c) Design a 2-bit magnitude comparator circuit whose outputs are J>K, J=K, J<K, Where J & K are 2-bit numbers. **[7]**

2. **(a)** Draw the Excitation Table of a J-K Flip Flop. **[2]**

(b) With a neat circuit diagram explain the function of 4:1 Multiplexer **[5]**

(c) Minimize the Boolean expression by K-Map & draw logic diagram of minimized expression by using Universal Gates. $F(P, Q, R, S) = \text{II}M(0, 1, 4, 5, 8, 13, 14,)$. IId (6, 9, 12) **[7]**

3. **(a)** What do you mean by min-term & max-term? What is the relation between them? **[2]**

(b) Design a combinational logic circuit for converting BCD to 7-segment decoder. **[5]**

(c) Explain working principle of Master Slave J-K Flip Flop with diagram. Why it is used? **[7]**

4. **(a)** State De-Morgan's law. **[2]**

(b) Whit necessary truth table and logic diagram construct a fill adder circuit. **[5]**

(c) Explain with neat sketch the working of a TTL 'NAND' gate circuit. **[7]**

5. **(a)** Draw the symbol and truth table of a three input NOR gate **[2]**

(b) With neat sketch explain the working of a 'Parallel in Serial Out' (PISO) shift Register. **[5]**

(c) With neat sketch explain the working of a clocked RS flip flop using NAND gates with a truth table. **[7]**

6. **(a)** Reduce the expression : $F(B, C, D) = \Sigma m(0, 1, 3, 4, 6) + \Sigma d(2, 5, 7)$. **[2]**

(b) Explain the working of 4-bit binary parallel adder with neat diagram. **[5]**

(c) How a J-K Flip Flop is converted to R-S Flip Flop, D Flip Flop and T Flip Flop? **[7]**

7. **(a)** What is the difference between combinational logic circuit and sequential logic circuit. **[2]**

(b) Design a mod-5 synchronous counter using J-K Flip Flop and implement it. **[5]**

(c) With neat circuit diagram explain the working of R-2R Ladder type DAC. **[7]**

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III / SEM / E & TC / 2017 (W) [11-12-2017, REG]

DIGITAL ELECTRONICS

Sub Code – **ETT-302**

Full Marks: 70

Time: 3 hours

Answer any **FIVE** questions

The figures in the right-hand margin indicate marks

1. (2+5+7=14)

a) Convert the following Binary numbers into Gray codes: (i) 1101011 (ii) 100010110

b) Design the operation of full adder with the help of truth table and circuit diagram.

c) Perform the following:

i. BCD addition of (679.6 + 536.8)

ii. Subtract $(25)_{10}$ from $(36)_{10}$ by 2's complements method.

2. (2+5+7=14)

a) Define don't care condition.

b) Which gates are referred to as Universal gates and why? How other gates can be realized Using NOR gates only?

c) Simplify the given expression using Karnaugh's map and draw the logic circuit, using NAND gate only, $F(a, b, c, d) = \Sigma m(4, 5, 6, 12, 14, 15) + d(3, 8, 10)$

3. (2+5+7=14)

a) What do you mean by MUX and DE-MUX?

b) Design a 3 : 8 decoder with neat circuit diagram?

c) Design a 2 bit magnitude comparator circuit whose outputs are X > Y, X = Y, X < Y, Where X and Y are 2-bit numbers.

4. (2+5+7=14)

a) What is race around condition and how it can be eliminated?

b) State and prove De-Morgan's theorems?

c) Explain the working of SR flip-flop. How it is converted to JK and D Flip-flops?

5. (2+5+7=14)

a) Simplify the Boolean expression $A+B[AC + (B + \bar{C})D]$

b) Explain the concept of Seven Segment Display.

c) Draw the circuit diagram of master slave JK flip-f1op. Explain it with a functional table

6. (2+5+7=14)

a) State two differences between a counter and a register.

b) Explain briefly SISO, PIPO and SIPO register.

c) With a suitable logic diagram and truth table design a synchronous decade counter.

7. (2+5+7=14)

a) Draw 2-input TTL NAND gate?

b) Explain the principle of working of R-2R ladder type DAC.

c) With neat diagram explain 4-bit ripple counter with its waveforms.

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III / SEM / E & TC / 2017(S) [13-07-2017, Instant]

DIGITAL ELECTRONICS

Sub Code – **ETT-302**

Full Marks: 70

Time: 3 hours

Answer any **FIVE** questions

The figures in the right-hand margin indicate marks

1. (a) Define modulus of a counter. [2
(b)Differentiate between Asynchronous and Synchronous counter. [5
(c)Which gates are referred to as universal gates and why? How other gates can be Implemented by using universal gates? [7

2. (a) What is Decoder and where it is used? [2
(b)With a neat diagram explain the operation of SIPO and SISO register? [5
(c) Design a synchronous 4 bit up counter using T-Flip Flop. [7

3. (a) Define Racing condition. [2
(b) Show the logic diagram of a clocked SR Flip-Flop. Explain its working with functional table
(c) Draw the logic circuit of full subtractor. Give its logic circuit with any one of universal gates.

4. (a) Define fan out and propagation delay. [2
(b) Explain the operation of seven segment display and LED. [5
(c) Design a 4 bit combinational logic circuit to produce 2's complement of the 4 bit binary no.

5. (a) State De-Morgan's theorem. [2
(b) Explain with logic diagram & functional table the working of a clocked SR Flip Flop. [5
(c) Simplify the expression by using K-map. F (A, B, C, D) = ∑m (4, 7, 12, 15) + d (0, 3, 8, 11) and implement it with NAND gate. [7

6. (a) Write down the truth table of a 2 input Exclusive - NOR gate. [2
(b) Differentiate between combinational and sequential logic circuit. [5
(c) Design a 2 bit magnitude comparator circuit. Whose outputs are A > B, A = B, A < B Where A and B are 2 bit numbers. [7

7. (a) Which code is known as self correcting code and why? [2
(b) Perform BCD addition of (204.6 + 185.56). [5
(c) Design a 8 : 3 Encoder. Give its logic expression and truth table. Implement the logic circuit with basic gates. [7

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III / SEM / E & TC / 2016 (W) [DEC, Reg]

DIGITAL ELECTRONICS

Sub Code – **ETT-302**

Full Marks: 70

Time: 3 hours

Answer any **FIVE** questions

The figures in the right-hand margin indicate marks

1. (a) Define Radix of a number system. [2
(b) Design a 2 : 4 decoder with neat circuit diagram. [5
(c) With neat circuit diagram explain the function of 1 : 4 Demux and 4 : 1 Mux. [7

2. (a) Why multiplexer are referred to as data selectors? [2
(b) Which gates are referred to as Universal gates and why? How other gates can be realized Using NOR gates only? [5
(c) Sketch the logic diagram of clocked JK Flip - Flop. Explain its working with functional table.

3. (a) State two differences between weighted and non-weighted binary codes. [2
(b) Simplify the Boolean expression y = $\overline{(A\bar{B}C)(\overline{A\bar{B}}) + BC}$ and draw the logic circuit using NAND gates only. [5
(c) Simplify the given expression using Karnaugh's map and draw logic circuit using universal Gates: F (a, b, c, d) = ∑m (4, 7, 12, 15) + d (0, 1, 2, 3, 8, 9, 10, 11) [7

4. (a) Define the term Resolution and Monotinicity. [2
(b) Distinguish between combinational and sequential logic circuit. [5
(c) Design a 2 bit comparator circuit whose outputs are A > B, A < B, and A = B Where A and B are each 2 bit numbers. [7

5. (a) Perform 1's complement subtraction of 00010 - 001111. [2
(b) Design the operation of full subtractor with the help of truth table and circuit diagram. [5
(c) Design and explain the working of a 4 bit Ripple counter with truth table and timing diagram.

6. (a) Convert (1011011) from gray to binary code. [2
(b) Find the complement of F = x + yz; then show that **F $\bar{F}$ = 0** and **F + $\bar{F}$ = 1**. [5
(c) Draw the circuit of master-slave JK Flip – Flop. Explain it with a functional table. [7

7. (a) Define Racing condition. [2
(b) Explain the operation of & segment display. [5
(c) Design a MOD – 10 Counter with a neat circuit diagram. [7

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III / SEM / E & TC / 2015 (W)

DIGITAL ELECTRONICS

Sub Code – **ETT-302**

Full Marks: 70

Time: 3 hours

Answer any **FIVE** questions

The figures in the right-hand margin indicate marks

1. (a) Define Modulators of a Counter. [2

(b) Describe the working of a SIPO shift register with the help of a suitable logic diagram. [5

(c) Discuss the operation of an asynchronous counter with its timing diagram. [7

2. (a) State de Morgan's theorem. [2

(b) With a neat circuit diagram explain the function of 1: 4 Demux circuits. [5

(c) Design a 2 bit magnitude comparator circuit whose outputs are X > Y, X = Y, X < Y, Where X and Y 2-bit numbers. [7

3. (a) Convert the following binary numbers into gray codes: **(i)** 1101011 **(ii)** 100010110 [2

(b) Explain the working of clocked RS Flip-flop with its functional table with neat diagram. [5

(c) Which gates are referred to as Universal Gates and why? How other gates can be Implemented by using any one of the universal gates? [7

4. (a) Which code is known as self correcting code and why? [2

(b) Design and describe 4 : 2 encoder. [5

(c) Simplify and minimize the 4 variable logic expression by using K – map and implement this circuit by using NOR gates. $F(A,B,C,D) = \pi M(0, 2, 4, 5, 6, 8, 9, 10, 12, 13, 14) + d(0, 2, 5)$.

5. (a) Find the 2's complement of a number 11001011. [2

(b) Simplify the Boolean expression by Boolean algebra and draw the logic circuit by using NAND gates. $X = AB + \bar{A}C + A\bar{B}C\,(AB + C)$. [5

(c) With a suitable logic diagram design a decade counter. Write its truth table too. [7

6. (a) What is a Multiplexer and Decoder? [2

(b) Explain the working of a Ladder network type D/A converter with diagrams. [5

(c) Design a combinational logic circuit for converting 4 bit binary to BCD code. [7

7. (a) State two differences between a counter and a register. [2

(b) Differentiate between Latches & Flip Flops & explain working of JK flip-flop with diagram.

(c) Covert the following: [7

i. JK FF to D FF

ii. SR FF to T FF

iii. JK FF to SR FF

iv. T FF to D FF

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III / SEM / E & TC / 2014 (W)

DIGITAL ELECTRONICS

Sub Code – **ETT-302**

Full Marks: 70

Time: 3 hours

Answer any **FIVE** questions

The figures in the right-hand margin indicate marks

1. (a) Subtract $(0111)_2$ from $(1111)_2$ by using 2's Complement method. [2
(b)State and prove De-Morgan's theorems. [5
(c)Which gates are referred as universal gates & how other gates can be realized by NAND gates

2. (a) Define don't care condition. [2
(b)Write SOP and POS form of Boolean expression. F (A, B, C) = Σm (0, 1, 3, 5, 7). [5
(c) Simplify the Boolean expression using K -Map SOP form,
F (A,B,C,D) =Σm (0, 1, 2, 3, 8, 9, 10, 11, 13, 15) & draw its logic circuit using NAND gate. [7

3. (a) Define combinational logic circuit. [2
(b) Explain briefly 1: 4 DEMUX with neat diagram and truth table. [5
(c) Explain briefly full adder logic circuit with neat diagram. [7

4. (a) Define race around condition. [2
(b) Explain the working of S-R flip-flop using NAND gates. [5
(c) Explain the-working of JK flip-flop. How it is converted to RS; T and D Dip-flops? [7

5. (a)Define Fan-in and Fan-out. [2
(b) Explain with neat sketch the working of 2-input NAND gate TTL logic family. [5
(c) Explain briefly the working of 4-bit asynchronous up counter with neat diagram? [7

6. (a) Draw CMOS logic circuit of NAND gate. [2
(b) Explain briefly about universal shift register with neat diagram. [5
(c) Explain briefly SISO, SIPO, PISO and PIPO register. [7

7. (a) Write the difference between weighed resistor DAC and R-2R DAC register. [2
(b) Explain briefly about weighted-register DAC with neat diagram. [5
(c) Explain briefly the working of Dual-Slope ADC. [7

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Collected By:-
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III / SEM / E & TC / 2013 (W)

DIGITAL ELECTRONICS

Sub Code – **ETT-302**

Full Marks: 70

Time: 3 hours

Answer any **FIVE** questions

The figures in the right-hand margin indicate marks

1. (a)What do you mean by Radix of a number? [2
(b)Which gates are referred to as Universal gates and how other gates can be realized using NAND gates? [6
(c)Simplify the given expression using Karnaugh's map and draw the logic circuit, using NAND gate only, $F(a, b, c, d) = \Sigma m (0,2,3,4,7,9,15) + d (6,8, 11)$ [8

2. (a)Convert (1110 110 I) from gray to binary code. [2
(b)Explain the operation of seven segment display. [6
(c) Design a 2 bit magnitude comparator circuit whose outputs are A > B, A = B and A < B Where A and B are two bit numbers? [8

3. (a)What is Racing Condition? [2
(b)Convert (**i**) SR to D flip-flop. (**ii**) JK to T flip-flop. [6
(c) Sketch the logic diagram of clocked RS flip-flop based on NAND gate. Explain its working with a functional table. [8

4. (a) Define the terms fan-in and fan-out. [2
(b)Design a 4 : 2 encoder with neat circuit diagram. [6
(c) With neat sketch explain the working of PISO register. [8

5. (a) What is a Register? State its use. [2
(b)Explain the binary weighted type of D/A converter with neat sketch. [6
(c) Design a synchronous 4 bit down counter using flip-flops. [8

6. (a) Perform 2's complement subtraction of 29 - 23. [2
(b) Distinguish between synchronous and asynchronous counter. [6
(c) Explain the working of dual slope type A/D converter with neat sketch. [8

7. (a) Define resolution of an 8 bit DAC. [2
(b)With neat sketch explain the working of a 2 bit TIL NAND gate. [6
(c)Draw the circuit diagram of master slave JK flip-f1op. Explain it with a functional table. [8

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III / SEM / E & TC / 2012 (W)

DIGITAL ELECTRONICS

Sub Code – **ETT-302**

Full Marks: 70

Time: 3 hours

Answer any **FIVE** questions

The figures in the right-hand margin indicate marks

1. (a) Convert $(105.25)_{10}$ into binary and hexadecimal number. [2

(b) Subtract $(25)_{10}$ from $(36)_{10}$ with the help of 1's and 2's complements method and write the advantages of 2's complement. [6

(c) Define univcrsa1 gates and realize other gates using Universal gates. [8

2. (a) What is the difference between weighted & non-weighted codes? Give example of each. [2

(b) With the Help of truth table and diagram, explain the operational of two input EX-OR gate. Realize EX-OR gate using NAND gates only. [6

(c) Minimize the following Boolean expression by K-map and draw the logic diagram of Minimized expression. $F = (A, B, C, D) = \Sigma m\ (0, 2, 4, 6, 10, 12, 15) + \Sigma d\ (l, 3, 7, 9, 11)$ [8

3. (a) Define SOP and POS in connection with Boolean algebra. [2

(b) Describe the operation of a Full-subtractor with the help of truth table find diagram. [6

(c) Explain the function of 1: 4 De-MUX with neat diagram and truth table. [8

4. (a)What is the difference between encoder and decoder? [2

(b) Explain the operation of a Two Bit Binary Comparator with truth table and logic diagram. [6

(c) With neat diagram, explain the operation of a J-K flip-flop and write its disadvantages. [8

5. (a) Convert $(11011)_2$ into gray code. [2

(b) Explain the different characteristics of logic family. [6

(c) Describe the operation of TTL NAND gate. [8

6. (a) What do you mean by a Flip-Flop? [2

(b) Describe the function of different types Shift Register briefly. [6

(c) Explain the working of a 4-Bit ripple counter with truth table and timing diagram. [8

7. (a) What is the difference between combination and sequential logic circuit? [2

(b) Explain the principle of working of R-2R ladder type DAC. [6

(c) Describe the function of a Dual slope ADC. [8

8. (a) What do you understand by LCD? [2

(b) Explain the concept of Seven Segment Display. [6

(c) Describe the function of Universal shift register with neat diagram. [8

---ALL THE BEST --- ALL THE BEST ---

III / SEM / E & TC / 2011 (W)

DIGITAL ELECTRONICS

Sub Code – **ETT-302**

Full Marks: 70

Time: 3 hours

Answer any **FIVE** questions

The figures in the right-hand margin indicate marks

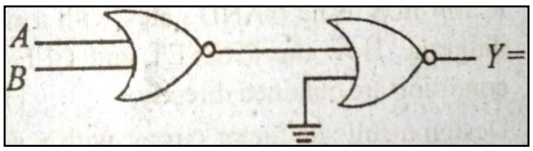
1. Answer ALL questions: [2 x10]

(a) What is meant by radix of a number system?

(b) Write first 8 numbers in octal system.

(c) What is race around condition and how it can be eliminated?

(d) What is the output of the following logic circuit? →



(e) What is modulus of a counter?

(f) Multiply $(1111001)_2$ by $(1001)_2$.

(g) $(17.75)_{10}$ = (_____) $_2$ = (_____) $_{16}$.

(h) What do you mean by serial data transfer?

(i) What do you understand by 1's and 2's complement of binary number?

(g)What is a flip-flop and how they can be classified?

2. Answer any SIX questions: [5 x 6]

(a) Which gates are called universal gates and how the other gates can be implemented by universal gates?

(b) Design a 4: 1 multiplexer circuit using logic gates and truth table.

(c) What is meant by Hamming code? Explain it with suitable example.

(d) Explain with neat sketch the working of a 2-input TTL NAND gate.

(c) Explain the working of a 4-bit SFSO register with the help of suitable circuit diagram.

(f) Simplify the Boolean expression: X =AB.AC+ABC. Also draw the logic circuit using NAND gates only.

(g) Explain the working of a 4-bit ripple counter to counter 16 states with neat circuit diagram.

(h) Explain the working of a full adder with neat diagram.

3. What are the various methods used for D/A conversion? Explain the working of a R-2R ladder. Network type D/A converter. [10

4. Simplify the logic function: F (A, B, C, D) = Σm (0, 2, 4, 6, 7, 8, 10, 12, 13 15) in both **SOP** and **POS** form using K-map. Implement the real minimal expression with basic logic gates. [10

5. Design a 2-bit magnitude comparator circuit and explain its operation. [10

6. Explain the working of Master-Slave J- K flip-flop using NAND gates with a neat diagram. How the PRESET and CLEAR condition are obtained directly. [10

7. (a) Design a Full Subtractor circuit with a neat diagram. [5

(b) Subtract $(1101)_2$ - (1001) using l's and 2's complement method. [5

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III / SEM / E & TC / 2010 (W)

DIGITAL ELECTRONICS

Sub Code – **ETT-302**

Full Marks: 70

Time: 3 hours

Answer any **five** questions

The figures in the right-hand margin indicate marks

[GROUP-A]

1. Answer all questions: [2 x 10

(a) Define radix.

(b) Convert the Decimal number $(1010)_{10}$ into Binary number. .

(c) Find the two's complement of a number $(10000000)_{2.}$

(d)Write down the truth table of 3-input XNOR gate.

(e) Convert (11101101) from gray to binary code.

(f) What is race-around condition and why it is essential?

(g) In a 14 pin IC DIP package how many 3 input NAND gates can be fabricated?

(h) Define flip-flop and name various types.

(i) Explain "Fan out" with reference to logic families.

(j)Write the difference between Asynchronous and synchronous circuit.

[GROUP-B]

2. Answer any **SIX** questions: [5 x 6

(a) State and prove De-Morgan's theorems.

(b) Construct a BCD full adder circuit with a neat sketch. .

(c) With neat sketch explain working of a clocked RS flip-flop using NAND gates with a truth table.

(d) Explain the working of a Ladder Network type D/ A converter with diagrams.

(e) With neat circuit diagram explain the function of l: 4 lines De-Mux circuit. .

(t) Design a full subtracter circuit using gates only.

(g) Using K-map, obtain minimum sum of product for the switching function given by
f (X, Y, Z, W) =Σ m(0, 1,. 3, 7, 8, 12) + Σd (5, 10, 13, 14) and implement using AOI gates.

(h) Explain with neat sketch the working of a C-MOS NAND gate circuit.

[GROUP-C]

Answer any THREE questions: [3 x 10

3. Design a 2-bit Magnitude comparator circuit whose output are A > B, A = B, A < B, where A and Bare 2-bit numbers.

4. With neat sketch explain the working of a Universal Shift Register.

5. Explain the working of a 4-bit ripple counter with truth table and timing diagram.

6. Design a seven-segment decoder circuit.

7. (a) Explain the principle and working of LCD and its type. [5

(b) Explain 1 's and 2's complement method of subtraction with example in each. [5

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